WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first polysilicon layer; and

a second polysilicon layer on the first polysilicon layer.

2. The semiconductor device of claim 1 wherein the first polysilicon layer and the second polysilicon layer are doped separately.

3. The semiconductor device of claim 1 wherein the first polysilicon layer and the second polysilicon layer comprise a top plate of a capacitor.

4. The semiconductor device of claim 3 wherein the capacitor is a storage capacitor of a memory cell.

5. The semiconductor device of claim 3 wherein the semiconductor device is on a die with a second semiconductor device having a single polysilicon layer.

6. The semiconductor device of claim 5 wherein the single polysilicon layer is formed in the same process step as one of the first polysilicon layer and the second polysilicon layer.

7. The semiconductor device of claim 1 wherein the first polysilicon layer and the second polysilicon layer comprise a gate of a transistor.

8. The semiconductor device of claim 7 wherein the transistor is an access transistor of a memory cell.

9. The semiconductor device of claim 7 wherein the semiconductor device is on a die with a second semiconductor device having a single polysilicon layer.

10. The semiconductor device of claim 9 wherein the single polysilicon layer is formed in the same process step as one of the first polysilicon layer and the second polysilicon layer.

11. A memory device having a cell region and a periphery region, the memory device comprising:

a first device formed in the cell region, the first device having an electrode having a first polysilicon layer formed above a second polysilicon layer, the first polysilicon layer electrically coupled to the second polysilicon layer; and

a second device formed in the periphery region, the second device having an electrode formed of a single layer of polysilicon.

12. The memory device of claim 11 wherein the first polysilicon layer of the first device is substantially the same thickness as the single layer of polysilicon of the second device.

13. The memory device of claim 11 wherein first polysilicon layer of the first device is formed in the same process step as the single layer of polysilicon of the second device.

14. The memory device of claim 11 wherein the second polysilicon layer of the first device is formed in the same process step as the single layer of polysilicon of the second device.

15. The memory device of claim 11 wherein the first device is a capacitor.

16. The memory device of claim 11 wherein the first polysilicon layer and the second polysilicon layer comprise a plate of the capacitor.

17. The memory device of claim 11 wherein the first device is a transistor.

18. A method of forming a semiconductor device, the method comprising:

forming on a substrate a first doped polysilicon layer; and

forming a second doped polysilicon layer on the first doped polysilicon layer.

19. The method of claim 18 wherein the first doped polysilicon layer is formed by in-situ doped poly deposited by a furnace process.

20. The method of claim 18 wherein the first doped polysilicon layer is formed of p-type doped polysilicon.

21. The method of claim 20 wherein the first doped polysilicon layer is doped with a material selected from the group consisting essentially of phosphorous, nitrogen, arsenic, and antimony.

22. The method of claim 18 wherein the second doped polysilicon layer is formed of p-type doped polysilicon.

23. The method of claim 22 wherein the second doped polysilicon layer is doped with a material selected from the group consisting essentially of phosphorous, nitrogen, arsenic, and antimony.

24. A method of forming a semiconductor devise, the method comprising:

forming a cell gate oxide in a cell region;

forming a logic gate oxide in a periphery region;

forming a first doped polysilicon layer on the cell gate oxide; and

forming a second polysilicon layer on the logic gate oxide and the first doped polysilicon layer.

25. The method of claim 24 wherein the second polysilicon layer positioned above the cell gate oxide is a p-type doped polysilicon.

26. The method of claim 25 wherein the second polysilicon layer is doped with a material selected from the group consisting essentially of phosphorous, nitrogen, arsenic, and antimony.

27. The method of claim 24 wherein the step of forming a first polysilicon layer is performed by depositing by furnace an in-situ doped polysilicon.

28. The method of claim 27 wherein depositing by furnace is performed at a temperature of about 540° C to about 640° C.

29. The method of claim 24 wherein the second polysilicon layer is formed of undoped polysilicon.

30. The method of claim 24 further comprising the step of doping the second polysilicon layer located above the cell gate oxide with a p-type dopant.

31. The method of claim 30 further comprising the step of doping the second polysilicon layer located above the logic gate oxide with an n-type dopant.

32. The method of claim 30 further comprising the step of doping the second polysilicon layer located above the logic gate oxide with a p-type dopant.

33. The method of claim 30 wherein the p-type dopant is selected from the group consisting essentially of phosphorous, nitrogen, arsenic, and antimony.